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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/148,392	09/04/98	BAEZ	F 042390.P5512

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EXAMINER	
THOMSON, W	
ART UNIT	**PAPER NUMBER**
2763	2

DATE MAILED: 03/21/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/148,392	Baez
Examiner	**Group Art Unit**
William Thomson	2763

☒ Responsive to communication(s) filed on *Sep 4, 1998*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-27* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-27* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-27 have been submitted for examination. Claims 1-27 have been examined and rejected.

TITLE

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title is of a generic nature drawn to a family of systems and not to the applicant's specific invention.

Specification

It is noted that this application appears to claim subject matter disclosed in prior copending Application No. 09/474,008, filed December 28, 1999. A reference to the prior application must be inserted as the first sentence of the specification of this application if applicant intends to rely on the filing date of the prior application under 35 U.S.C. 119(e) or 120. See 37 CFR 1.78(a). Also, the current status of all nonprovisional parent applications referenced should be included.

ABSTRACT

3. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and *should include that which is new in the art to which the invention pertains*. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, *the abstract should include the technical disclosure of the improvement*. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. *If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.*

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Double Patenting

4. Claims 1-27 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-30 of copending Application No. 09/474,008. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Sarin or Jyu et al. and rejected under 102(a) as being clearly anticipated by Roethig(145) and rejected under 102(b) as being clearly anticipated by Breid.

Taking claim 1, for example, Sarin and Jyu et al. and Roethig(145) and Breid disclose:

A method for determining optimal values of design parameters of a subsystem comprising a plurality of circuits, the method comprising: (Abstracts, Figures and related sections, Detailed Description of Invention sections)

creating parameter functions for the corresponding circuits, the parameter functions representing a relationship among the design parameters; and

optimizing the design parameters based on the parameter functions to satisfy the design constraints.

As to claim 2, the method of claim 1, wherein the creating the parameter functions comprises:

configuring each circuit of the plurality of circuits and generating values of design parameters for each circuit according to the configuration circuit, the values providing the parameter functions are discloses throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 3, the method of claim 2, wherein the design parameters include constraint and optimizing sets, the constraint set including constraint parameters having values selectable to meet the design constraints, the optimizing set including optimizing parameters having values to be optimized are disclosed throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 4, the method of claim 3, wherein optimizing comprises:

selecting values of the constraint parameters to meet the design constraints;

determining values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

iterating the selection of values and determining of values steps until values of the optimizing parameters are within a predetermined optimal range are disclosed throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 5, the method of claim 3, wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter are disclosed throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 6, the method of claim 5, wherein the design constraints include a delay constraint are disclosed throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 7, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes sizing components in each circuit is disclosed throughout Sarin and Jyu et al. and Roethig(145) and Breid.

As to claim 8, the method of claim 6, wherein the step of configuring each circuit of the plurality of circuits includes selecting a design technology for each circuit, the design technology being one of static and dynamic technologies is disclosed throughout Sarin and Jyu et al. and Roethig (145) and Breid.

As to claim 9, the method of claim 7, wherein the generating values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions including generating a circuit netlist representing the configured circuit;

generating a timing file based on the circuit netlist using a circuit critical path;

calculating timing values by using a timing simulator; and

calculating power values by using a power estimator is disclosed throughout Sarin and Jyu et al. and Roethig (145) and Breid.

As to claim 10, the method of claim 8, wherein optimizing comprises:

selecting values of the delay parameter within the delay constraint;

determining values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and

iterating the steps of selecting values and determining values until values of the power parameter are within a predetermined optimal range are disclosed throughout Sarin and Jyu et al. and Roethig (145) and Breid.

As for claims 11-27 are rejected for the same reasoning as claims 1-10, set forth above, *supra*.. Claims 11-27 are equivalent machine readable medium having embodied a computer program for processing by a machine and system claims containing the same limitations and variations of limitations as recited in method claims 1-10.

Conclusion

Applicant is currently claiming a system which uses timing or propagation delays and power parameters to optimize transistor sizing. The relationships between these two parameters and the sizing of a circuit are well known in the art. The use of a computer system to optimize the layout and sizing of the circuit based on these parameters is just as old in the art. Graphical and curve trace methodologies for optimizations that cover applicant's claimed invention go back for many years.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration needs to be given to the following art, prior to applicant's response to Examiner's Office Action.

U.S. Patent 5,500,805 issued to Lee et al. discloses a circuit design system and method including optimizing using power and delay times as parameters.

U.S. Patent 5,835,380 issued to Roethig discloses a simulation based extractor of expected waveforms for gate-level power analysis tool.

U.S. Patent 5,926,396 issued to Ohara discloses logic synthesis method, semiconductor integrated circuit and arithmetic circuit.

U.S. Patent 5,774,367 issued to Reyes et al. discloses a method of selecting device threshold voltages for high speed and low power.

U.S. Patent 5,889,685 issued to Ramachandran discloses a method and apparatus for automatically characterizing short circuit current and power consumption in a digital circuit.

U.S. Patent 5,917,729 issued to Naganuma et al. discloses a method of and apparatus for placing and routing elements of semiconductor integrated circuit having reduced delay time.

U.S. Patent 5,612,892 issued to Almulla discloses a method and structure for improving power consumption on a component while maintaining high operating frequency.

U.S. Patent 5,555,201 issued to Dangelo et al. discloses a method and system for creating and validating low level description of electronic design for higher level behavior oriented

description including interactive system for hierarchical display of control and data flow information.

U.S. Patent 5,910,898 issued to Johannsen discloses circuit design methods and tools.

U.S. Patent 5,666,288 issued to Jones et al. discloses a method and apparatus for designing an integrated circuit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Thomson whose telephone number is (703) 305-0022. The examiner can be usually reached between 9:30 a.m. - 4:00 p.m. Monday thru Friday. Voice mail is checked throughout the day. Please leave a detailed message.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Kevin Teska, can be reached on 704-305-9704. The fax phone number for this Group is 703-308-1396.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 703-305-3900.

William D. Thomson

Patent Examiner

A.U. 2763

March 7, 2000

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER